# Comprehensive Physical Model of Dynamic Resistive Switching in an Oxide Memristor

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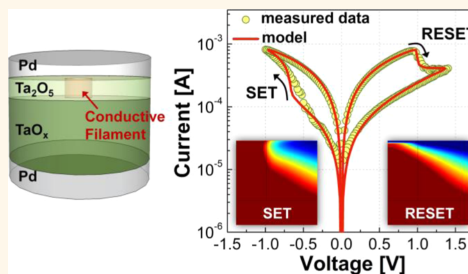
**ABSTRACT** Memristors have been proposed for a number of applications from nonvolatile memory to neuromorphic systems. Unlike conventional devices based solely on electron transport, memristors operate on the principle of resistive switching (RS) based on redistribution of ions. To date, a number of experimental and modeling studies have been reported to probe the RS mechanism; however, a complete physical picture that can quantitatively describe the dynamic RS behavior is still missing. Here, we present a quantitative and accurate dynamic switching model that not only fully accounts for the rich RS behaviors in memristors in a unified framework but also provides critical insight for continued device design, optimization, and applications. The proposed model reveals the roles of electric field, temperature, oxygen vacancy concentration gradient, and different material and device parameters on RS and allows accurate predictions of diverse set/reset, analog switching, and complementary RS behaviors using only material-dependent device parameters.




**KEYWORDS:** memristor · physical model · drift · diffusion · oxygen vacancy

The rapid advances in digital electronic devices in the past few decades have brought significant changes to society. Generally, digital devices such as field-effect transistors can retain two discrete stable states, "0" and "1", and fast and abrupt transitions between the two states have been regarded as an essential prerequisite for reliable device operation. However, as power consumption becomes a major bottleneck for current digital computing systems based on the von Neumann architecture, alternative computing technologies have begun to attract attention in recent years, such as neuromorphic systems and analog arithmetic computing schemes. Neuromorphic computing is a bioinspired approach that could be more energy-efficient than the conventional Boolean logic computation due to its parallelism, while offering other attractive features such as fault tolerance.[1−5] Additionally, arithmetic operations based on analog memories also present an attractive computation paradigm to complement digital von Neumann computations in the future.[6]

Memristors are two-terminal electrical devices whose resistances are modulated through the dynamic evolution of a set of internal state variables.[7−9] They have been extensively studied for nonvolatile memory storage, neuromorphic computing, and implementation logic applications.[4,5,10−13] However, although a number of models have been proposed to describe the device behavior, they are either nondynamic and can only predict steady-state properties[14] or oversimplified.[9,15−19] Providing a dynamic memristor model that can accurately explain the rich memristive switching behaviors not only fills an urgent need that enables accurate simulation of large-scale memristor systems but also can significantly improve our understanding of the different factors that drive the switching process and will be critical for continued optimization and design of this important class of devices.

In this work, we present a complete physical model that quantitatively and accurately describes the rich memristive switching behaviors in a tantalum-oxide-based bilayer memristor. As memory devices, tantalum-oxide-based memristors have shown excellent switching performance between two discrete resistance levels, including

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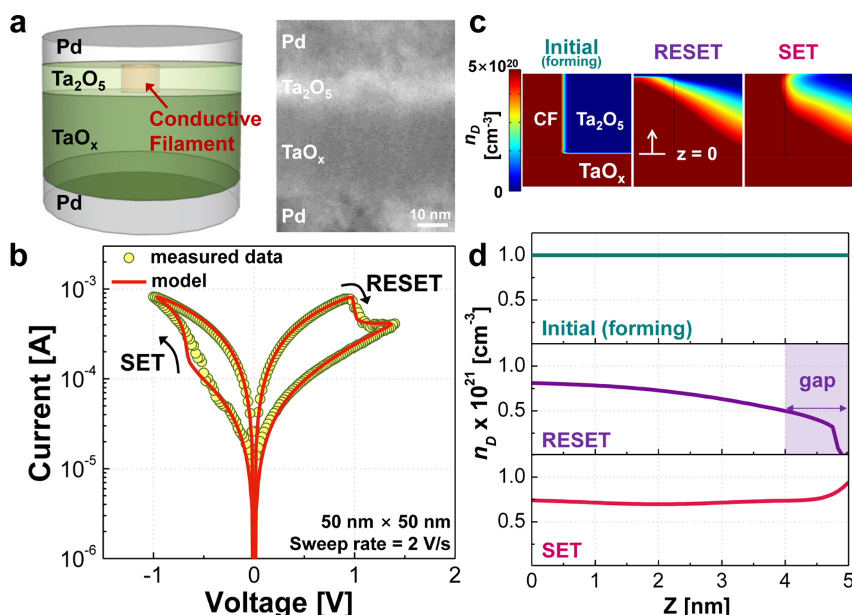


**Figure 1. Modeling a tantalum oxide memristor during set/reset. (a) Schematic and cross-sectional TEM images of the Pd/$Ta_2O_5$/$TaO_x$/Pd bilayer memristor device. (b) Measured and calculated DC *I*−*V* characteristics of the Pd/$Ta_2O_5$/$TaO_x$/Pd device. The measured device size is 50 nm × 50 nm, and the voltage sweep speed is 2 V/s. (c) Calculated 2-D maps of $n_D$ as well as (d) 1-D profiles of $n_D$ along the center of the CF in the initial state, after reset, and after the set process. The depleted gap is defined as the position where $n_D$ is below 5 × $10^{20}$ $cm^{-3}$. The $z = 0$ position is the $Ta_2O_5$/$TaO_x$ interface.**

extreme cycling endurances of over $10^{12}$ cycles and fast switching speeds below 10 ns.[20,21] By solving the dynamic transport equations of oxygen vacancies, we can precisely predict the resistive switching behaviors in tantalum-oxide-based memristors in both DC and pulse operation modes using a single set of material-dependent parameters. More importantly, analog switching behaviors were also observed in the simulation and confirmed experimentally. Our quantitative analysis reveals that the SET process is driven by both the electric field and thermal effects, while RESET is mainly driven by thermal effects. Furthermore, rich dynamic switching processes including complementary resistive switching (CRS) and different analog switching properties in the memristor can be fully accounted for by considering the competition of diffusion, drift, and thermophoresis effects, using only one set of material-specific parameters.

## RESULTS AND DISCUSSION

The tantalum-oxide-based bilayer memristor consists of a highly resistive $Ta_2O_5$ layer on top of a less resistive $TaO_x$ base layer (see Supporting Information) sandwiched by top and bottom Pd electrodes (TE and BE),[22] as shown in Figure 1a. To explain the resistive switching behaviors, the concept of the formation/rupture of conductive filaments (CFs) has been generally accepted.[23] Here the filaments correspond to regions with high oxygen vacancy ($V_O$) concentration so the local electrical conduction becomes metallic.[24] The device can be set (from a low conductance state to a high conductance state) or reset (from a high conductance to a low conductance) among different resistance states by controlling the properties (*e.g.*, $V_O$ concentration and shape) of the filament. The simulation starts immediately after the electroforming process, where a continuous CF has connected the TE and $TaO_x$ layer (Figure 1c). The dynamic resistance switching processes are driven by $V_O$ migration through three factors: the local electric field, the $V_O$ concentration gradient, and the temperature gradient due to Joule heating.[23−25] Thus, the complete memristive switching process can be captured after self-consistent solving three partial differential equations (PDEs) following an approach first proposed by Ielmini *et al.*:[19,25,26] (1) a drift/diffusion continuity equation for $V_O$ transport (Supporting Information eq 1), (2) a current continuity equation for electrical conduction (Supporting Information eq 2), and (3) a Fourier equation for Joule heating (Supporting Information eq 3), as summarized in Figure S2. These three PDEs were self-consistently solved here through a numerical solver (COMSOL) to calculate the $V_O$ concentration $n_D$, electrostatic potential $\psi$, and local temperature $T$. The details for the proposed model are discussed in Supporting Information (Figures S2−S4).

Figure 1b shows the measured and calculated DC *I*−*V* characteristics during the set and reset processes. The reset transition starts near 0.9 V. The resistance gradually increases and finally reaches a resistance roughly one decade higher after reset. Similarly, the set transition occurs at a negative voltage and recovers the original lower resistance. Both the calculated reset and set processes are accurately captured by

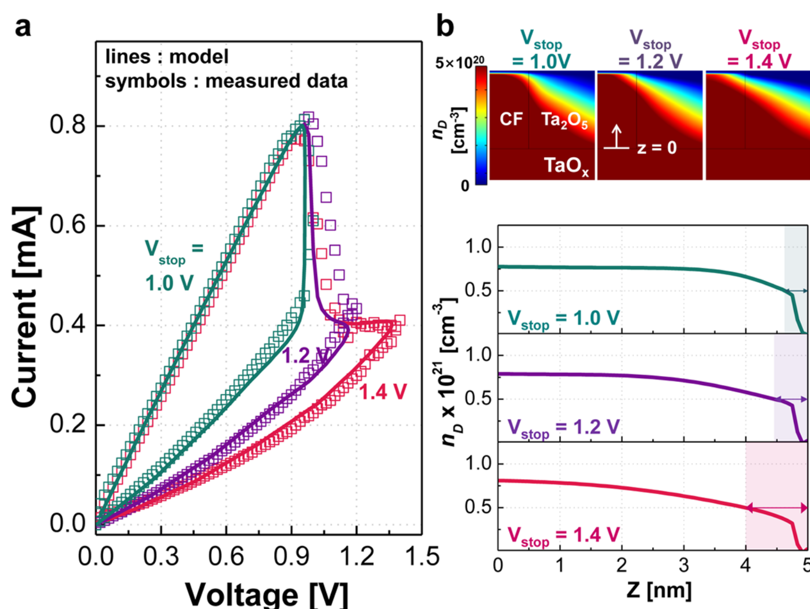


**Figure 2. Gradual reset process. (a) Measured and calculated *I*−*V* curves, showing the reset transition, obtained by varying $V_{stop}$ (1.0, 1.2, and 1.4 V). The measured device size is 100 nm × 100 nm, and the voltage sweep speed is fixed to 2 V/s. (b) Calculated 2-D maps of $n_D$ as well as 1-D profiles of $n_D$ corresponding to the different $V_{stop}$ values.**

the model, as shown in Figure 1b. The physical nature of the set and reset processes can be studied by examining the $n_D$ profiles, as shown in Figure 1d. Specifically, a gap of ∼1 nm with a depleted $V_O$ concentration was formed near the TE during reset, leading to the increase of the device resistance, while refilling the gap during set leads to the recovery of the high conductance. In addition, by controlling the maximum reset voltage $V_{stop}$, different resistance values can be obtained and have been measured experimentally, as shown in Figure 2a. The model accurately reproduces the gradual reset transition behavior with different values of $V_{stop}$ and reveals that the different resistance levels when using different $V_{stop}$ corresponds to the modulation of the length of the depleted gap,[10,25] as shown in Figure 2b. The ability to obtain different resistance values is necessary for multilevel storage in memory applications and for emulating analog weights in neuromorphic computing. By accurately capturing the resistive switching behaviors, the model further reveals the key enabling factors for multilevel switching. Specifically, the effects of different material and device parameters, for example, the TE material, oxide thickness, the activation energy $E_a$, and characteristic hopping distance $a$ for $V_O$ migration, have been thoroughly examined (see Supporting Information).

By accurately capturing the internal device dynamics, the proposed model not only reproduces the DC characteristics but also accurately captures time-dependent AC characteristics using the same set of material-dependent parameters. Below we show the experimental and simulation results focusing on pulse-programmed analog switching behaviors. Figure 3a shows the schematic of the pulse trains used for the measurements. Each pulse train consists of 20 set or reset pulses (−0.9 and 1.1 V, respectively) followed by small, nonperturbative read voltage pulses (0.2 V, 1 ms) in the intervals. Figure 3b shows the measured and the simulated conductance values during the applied pulse trains (the measured transient responses as a function of time is shown in Figure S5). A gradual transition in both the set and reset responses is clearly observed as the number of applied pulse increases, which is distinct from the previously discussed abrupt resistive switching behaviors in tantalum oxide.[20] The simulated results for the analog switching behavior also match very well with the measured data for both the set and reset pulse trains.

The accurate model allows us to gain insight into the factors affecting analog switching in oxide memristor devices. Figure 3c shows the calculated 2-D maps of $n_D$, and Figure 3d shows the calculated temperature $T$ and $V_O$ drift velocity $v$ at the center of the filament, at different points during the consecutive set/reset pulses. First, an abrupt transition occurs within the third set pulse (states A−C). At the starting point of the set period, the temperature inside the CF is lower than that reached during the reset pulse since the filament is not yet complete. Nevertheless, a sizable temperature increase may still be achieved locally (*e.g.*, local temperature of 500−600 K shown in Figure 3d). Consequently, the $V_O$ drift velocity $v$ is significantly enhanced due to both the strong electric field localized inside the depleted gap and the temperature increase. As a result, the refilling of the gap is dominated by the vertical $V_O$ drift flux. However, after the CF is completed at state C, the drift velocity $v$ quickly decreases due to the reduction of the electric field. Nevertheless, the

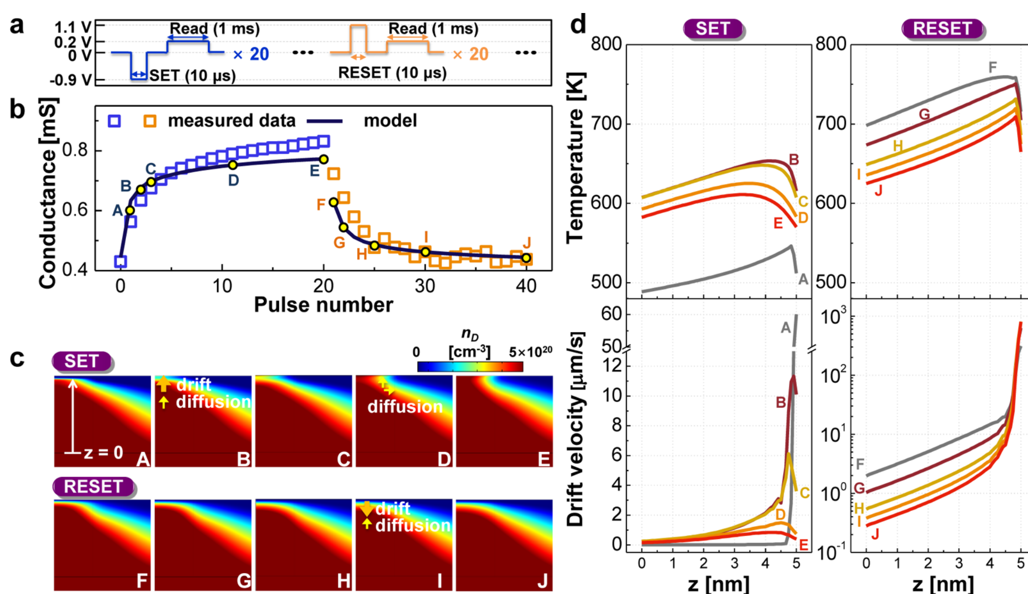


**Figure 3. Analog switching behaviors. (a) Schematics of the applied pulse trains used for the measurement of analog switching behavior. Each pulse train consists of 20 set or reset pulses (−0.9 and 1.1 V, 10 $\mu$s) followed by small, nonperturbative read voltage pulses (0.2 V, 1 ms) in the intervals. (b) Measured and calculated device conductance changes, where the conductance was measured during the read pulse and plotted as a function of applied pulse number. (c) Calculated 2-D maps of $n_D$ and (d) $T$ and $v$ at different points in the consecutive pulse trains (set pulses are states A−E, reset pulses are states F−J).**

continued $V_O$ diffusion flux allows the diameter of the CF to increase continuously during subsequent set pulses (states D and E, Figure 3c). Accordingly, the internal $V_O$ distribution of the CF follows a two-step process during the set process: (1) initial vertical gap filling by the field and thermal-driven migration of $V_O$ and (2) subsequent lateral expansion of the CF by diffusion. In addition, the depleted gap is localized at the point of maximum temperature, which depends on the structure of the device (whether it is a bilayer or single-layer memristor) and/or the thermal properties of the TE material.[26] In the case of the tantalum oxide bilayer memristor, the position near the TE is the hottest point during reset, and consequently, the depleted gap originates at this location during reset and is refilled during set, while the rest of the device regions experiences relatively little changes (Figure 3c).

A more gradual transition was also observed during reset (states F−J). Since the CF is initially connected during reset, the local temperature inside the filament can increase significantly due to Joule heating. This high temperature leads to simultaneous increases in both the drift and diffusion fluxes, but these two processes tend to have opposite directions during reset. Consequently, although the $V_O$ drift velocity $v$ is 10 times greater in the reset process than in the set process (Figure 3d) due to the higher temperature, a more gradual transition occurs during the reset process because the drift and diffusion fluxes partially cancel each other. In other words, to optimize the analog switching behavior, tuning the balance between the drift and diffusion fluxes is crucial.

In particular, sudden $V_O$ migration will occur during reset when this balance is disrupted and one flux becomes much larger than the other, and abrupt resistance switching instead of analog switching behavior will occur. In contrast, during set, the drift and diffusion fluxes have the same direction which normally leads to sharp switching. The accurate device model further allows us to examine the different factors driving the switching process. The $V_O$ drift and diffusion fluxes are determined by the diffusion coefficient ($D$) and drift velocity ($v$), respectively. These values are in turn functions of the characteristic hopping distance ($a$), with $D$ and $v$ (at high field) proportional to $a^2$ and $a\cdot\sinh(a)$, respectively (Figure S2). Therefore, the drift flux is more sensitive to the hopping distance and becomes larger than the diffusion flux as $a$ increases (Figure 4c), leading to more abrupt switching behaviors during the set and reset pulses. Figure 4d shows the calculated analog switching behavior at different values of $a$. Both the DC switching behaviors (Figure 4a) and pulse programming characteristics show distinctive differences between the device having the smallest $a$ (0.1 nm) which shows clear gradual (*e.g.*, analog) changes and the device having the largest $a$ (0.2 nm) which shows essentially binary (*e.g.*, digital) resistive switching. Additionally, because both the drift and diffusion fluxes increase with $a$, a switching material with larger $a$ will yield a wider gap during the reset process and more lateral expansion during the set process (Figure 4b). As a result, a larger dynamic range (on/off ratio) can be obtained for devices having higher $a$ values. It is clear from these

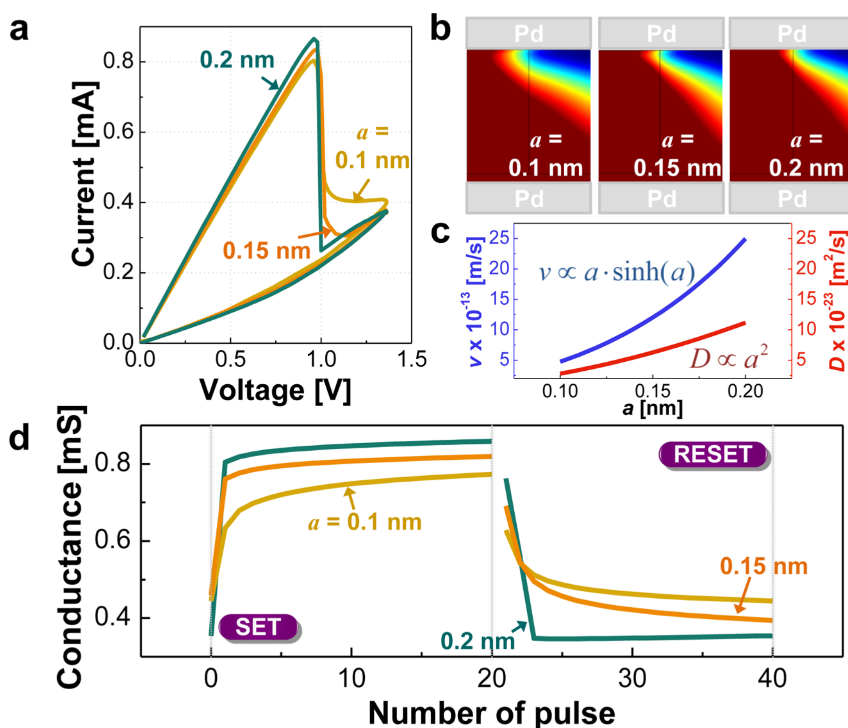


**Figure 4. Hopping distance effects on analog switching. Calculated (a) DC $I-V$ characteristics, (b) 2-D maps of $n_D$ after the set process. (c) Diffusion and drift components $D$ and $v$ as a function of the hopping distance $a$ under a high electric field ($10^7$ V/cm), and (d) analog switching behavior at different values of $a$.**

discussions that, by tuning the material properties, particularly the characteristic hopping distance *a*, different switching dynamics can be obtained, with a large *a* resulting in larger resistance ratios and more abrupt switching, while a small *a* is preferred to obtain a more gradual transition.

Based on the simulation results, guidance to device design can be obtained by examining the relevant device parameters. For example, besides the effect of the hopping distance *a*, the thermal properties of the TE (*i.e.*, the thermal conductivity $k_{th}$) also affect the analog switching behavior. As shown in Figure S6, as the $k_{th}$ of the TE increases, the heat generated by Joule heating can be easily dissipated through the TE, so the location of the depletion gap in the CF, that is, the location of the maximum temperature, is moved closer to the TE/$Ta_2O_5$ interface (Figure S6b). In addition, the maximum temperature is also decreased by effective heat dissipation through the TE (Figure S6c). Consequently, both the drift and the diffusion fluxes are decreased, and a more gradual transition during the set process is observed. If however an abrupt set process is desirable for memory applications, a TE material with low $k_{th}$ will be preferred. The effects of the oxide thickness and the activation energy $E_a$ are discussed in Supporting Information, as well.

One potential application of the analog memristor devices is neuromorphic computing by emulating synaptic components. Synaptic connections dominate the architecture of biological networks and are crucial to perception and learning. An important synaptic learning rule is known as spike-timing-dependent plasticity (STDP),[27] which regulates the synaptic weights based on the relative spike timings of the presynaptic and postsynaptic neurons. The ability to emulate STDP learning in nanoelectronic synapse devices will enable memristor-based, brain-inspired neuromorphic computational systems.[4,5,13] Below we show possible pulsing schemes for implementing STDP for tantalum-oxide-based memristors (Figure 5a). The prespike voltage ($V_{pre}$) and postspike voltage ($V_{post}$) are applied to the TE and the BE of the memristor, respectively. The net programming voltage ($V_{pre} - V_{post}$) is applied across the device at the moments of positive or negative $\Delta t$. $V_{min}$ and $V_{max}$ are the minimum and maximum voltage amplitudes that can induce potentiation (set) and depression (reset) across the synapse (memristor), respectively. Figure 5b shows the simulated conductance change rate based on the accurate physical model as a function of the relative timing of the pre- and postspike voltage applications, with different $V_{min}$ or $V_{max}$. It should be noted that this pulsing scheme is one of many possible ways to obtain STDP characteristics in memristors.[4,5,28] The simulated STDP characteristics are indeed consistent with the biological data measured in hippocampal glutamatergic synapses by Bi and Poo[27] or in other previous studies.[4,5,13,28] The accurate physical model proposed in this work thus will enable simulation of large-scale memristor-based neuromorphic systems and help

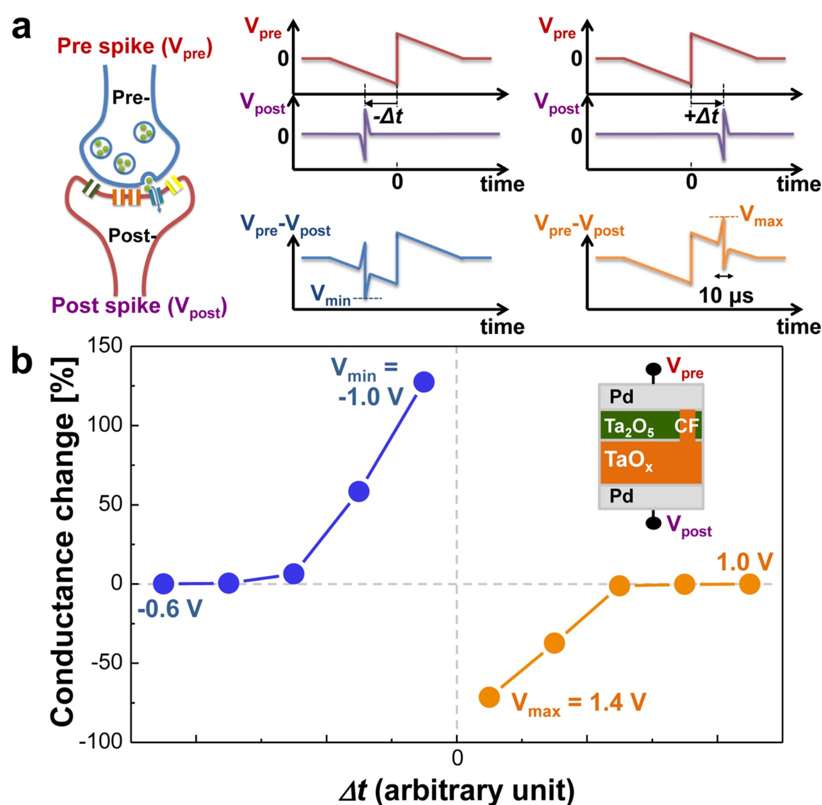


**Figure 5. Achieving STDP with the tantalum oxide memristor. (a) One possible pulsing scheme to implement STDP for tantalum-oxide-based memristors. (b) Simulated conductance change as a function of the relative timing of pre- and postspikes.**

continued improvement for designing appropriate materials or structures of synaptic devices.

Finally, we show that our proposed model can be used to describe the rich dynamic effects observed in memristors. One such example is the recently observed complementary resistive switching (CRS) behavior which leads to a decrease in current at higher voltages due to depletion of $V_O$ at a different location in the oxide stack.[29,30] It is known that both the bipolar switching and the CRS behaviors can be obtained from tantalum oxide memristors, depending on the $TaO_x$ base layer stoichiometry.[19,31] When the $TaO_x$ base layer is very oxygen-poor, the device exhibits typical bipolar switching, as shown in Figure 1b. In this case, the $TaO_x$ base layer contains a high concentration of $V_O$ and can act as an infinite reservoir of $V_O$. Consequently, resistive switching (in other words, the formation/rupture of the CF) occurs only inside the $Ta_2O_5$ layer. On the other hand, when the $TaO_x$ base layer is only moderately oxygen-poor, the $TaO_x$ base layer can no longer serve as an infinite $V_O$ reservoir and formation/rupture of the CF in the $TaO_x$ base layer is also possible, as depicted in Figure 6b. To simulate the CRS behavior, the initial $V_O$ concentration was assumed to be $n_D = 1 \times 10^{21}$ cm$^{-3}$ in both the $Ta_2O_5$ and $TaO_x$ layers, and the model successfully captures the CRS behavior (Figure 6a).

The nature of the CRS switching was revealed by the model by examining the distribution of $n_D$ at the different states of the device (*e.g.*, A, B, C, D, and E depicted in Figure 6a) (Figure 6c). When the device is in state A, a $V_O$ depletion gap is formed inside the $Ta_2O_5$ layer, so the overall conductance of the device is low. At negative voltages below −1 V, $V_O$ migration leads to the completion of the conducting path and causes the overall conductance to increase, and the device reaches the intermediate, high conductance state B. However, at even higher negative voltages, a depletion gap is developed near the BE and the device is switched to another low conductance state C. Both states A and C show similar high resistances but represent different internal states, as represented by the locations of the depletion gap and shown in Figure 6c. A similar process also occurs at positive biases, involving states D and E. These studies, using only one set of parameters at different conditions, further reveal the rich switching dynamics in memristors and the importance of the complete physical model covering the dynamic evolution of the CF.

## CONCLUSION

By solving the local electric field, temperature, and $V_O$ concentration self-consistently, we developed a complete and accurate physical model that quantitatively explains the dynamic memristive switching process. Significantly, the model reveals that the conducting filament is ruptured and formed locally inside

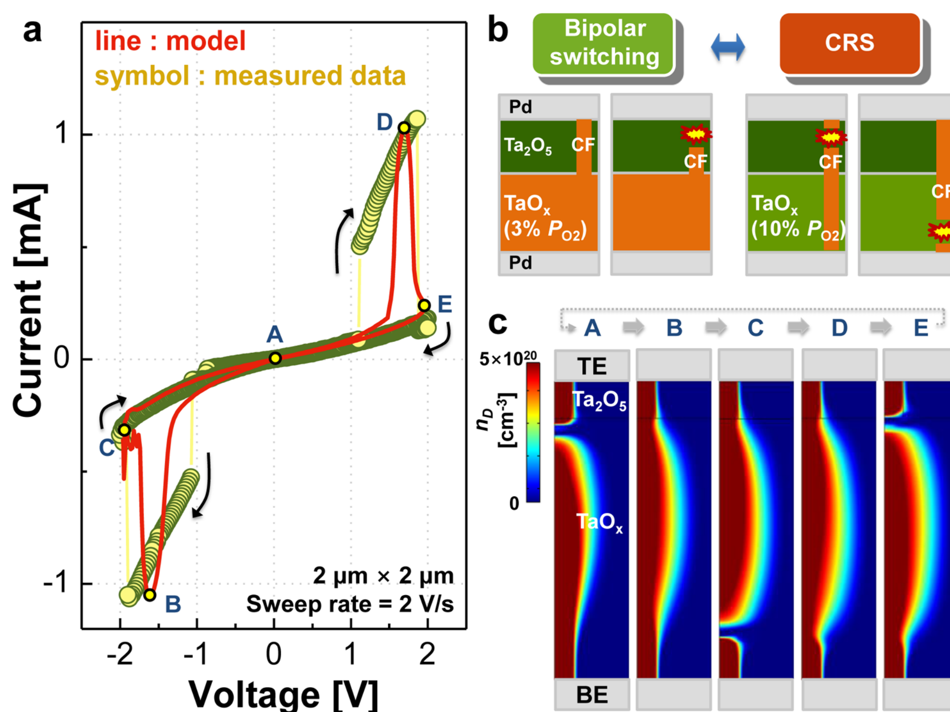


**Figure 6. Complementary resistive switching behavior. (a) Measured and calculated CRS behavior when 10% the oxygen partial pressure ($P_{O_2}$) during the reactive sputtering process was used during $TaO_x$ sputtering. The measured device size is 2 $\mu$m × 2 $\mu$m. In CRS simulation, activation energy for conduction ($E_{AC}$) of $Ta_2O_5$ is changed from 0.05 to 0.07 eV to provide a better fit with the experimental data. (b) Schematics explaining the evolution between bipolar switching and CRS for the different $P_{O_2}$ values. (c) Calculated 2-D maps of $n_D$ at different bias points (A, B, C, D, and E) depicted in (a).**

the switching layer, and the set process involves field and thermal-driven filament formation followed by filament expansion, while the reset process is dominated by thermal-driven filament rupture followed by gap widening. The competition between the drift and diffusion components during reset can lead to different resistive switching characteristics. Differences in material properties (*i.e.*, hopping distance), device layout, and electrode selection can also affect the device performance, and the role of thermal effects can be significant. The proposed model allows accurate prediction of resistive switching characteristics for both DC and AC input signals and was able to reproduce the analog switching and CRS behaviors. We believe such in-depth analysis of the memristive switching process not only provides a reliable and accurate physical picture of the resistive switching process but also produces much-needed guidelines for continued design and optimization of this important class of devices for memory and logic applications.

## METHODS

**Device Fabrication.** The memristor devices in this work with sizes ranging from 50 nm to 2 $\mu$m were fabricated in a crossbar structure on $SiO_2$ (100 nm)/Si substrates with electrodes patterned using either e-beam lithography (Raith 150) or traditional photolithography (GCA AS200 AutoStep). First, the bottom Pd electrode was deposited by e-beam evaporation followed by lift-off processes. Next, the $TaO_x$ base layer was deposited by direct current (DC) reactive sputtering of a Ta metal target in an $Ar/O_2$ gas mixture at 400 °C. The total pressure of $Ar/O_2$ was ~5 mTorr, and the oxygen partial pressure in the $Ar/O_2$ mixture was varied in the range of 3−10% in order to modulate the switching behavior of the devices. The $Ta_2O_5$ switching layer was then deposited by RF sputtering using a $Ta_2O_5$ ceramic target at room temperature in Ar with a pressure of ~5 mTorr. The top Pd electrode was then deposited by e-beam evaporation followed by lift-off processes. Finally, a reactive ion etching process using $SF_6$/Ar was performed to expose the bottom contacts. Figure S1 shows resistive switching behavior of the fabricated devices during forming, reset, and set steps. For the forming step, a resistor (5 kΩ) is serially connected with the device to prevent permanent breakdown.

*Conflict of Interest:* The authors declare no competing financial interest.

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*Supporting Information Available:* Additional discussions about the detail model derivation steps and other parameters related to the resistive switching behavior. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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